UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,289	04/01/2004	Bon-Woong Koo	012-2003	8581

7590 02/08/2006

Mark Superko
Varian Semiconductor Equipment Associates, Inc.
35 Dory Road
Gloucester, MA 01930-2297

EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/816,289	KOO ET AL.
	Examiner	Art Unit
	Terrence R. Willoughby	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 4/1/2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the following informalities: Figures 1, 4, 5 does not clearly show a plurality of channels (62,64,66) and a plurality of lifting pins (52,54,56) in reference to the drawing figures. The corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11,13,14,19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichelderfer, et al. (US 5,016,332) and in further view of Lubomirsky et al. (US 2002/0121312 A1).

Regarding claim 1, Reichelderfer et al. discloses an apparatus for handling a workpiece during semiconductor processing (column 1, lines 1-2, lines 17-21), comprising: a wafer platen (Fig. 3, 23) including a plurality of channels (44) each extending from a top surface to a bottom surface of the wafer platen (Fig. 2,14); a plurality of lift pins (Fig. 3,43) in alignment with the channels (44 and column 2, lines 28-30); and a mechanism for engaging the lift pins for lifting the workpiece away from the platen(Fig. 3,49 and column 2, lines 30-35), and a clamping for placing the workpiece in a position so that desired semiconductor processes may be performed to the workpiece through use of a locator pins (51). However, Reichelderfer et al. does not disclose explicitly a loading position of the workpiece on the wafer platen and a lift off position for removing the workpiece from the wafer platen after the desired semiconductor processes are completed.

However, Lubomirsky et al. discloses a loading position of the workpiece on the wafer platen (paragraph [0002], lines 13-17), a clamping position for placing the workpiece in a position so that desired semiconductor processes may be performed to

the workpiece (paragraph [0003], lines 1-5), and a lift off position (paragraph [0003], lines 5-11) for removing the workpiece from the wafer platen after the desired semiconductor processes are completed. It would have been obvious to those skilled in the art at the time the invention was made to have provided a mechanism for engaging the lifting pins between the wafer and wafer platen in a loading, clamping, and lift off position taught by Lubomirskey et al. for handling a workpiece or wafer taught by Reichelderfer et al. to provide a reliable mechanism for engaging the lifting pins on the surface of the wafer platen by carefully controlling the actuation of the lifting pins to avoid contact between the wafer and the platen to limit defects, and damage, such as wafer breakage as a result of unpredictable movement of the platen and to improve access to the wafer for easy handling insertion and removal.

Regarding claim 2, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the mechanism places the lift pins below the surface of the wafer platen in the load position (Lubomirskey et al., paragraph [0002], lines 13-17).

Regarding claim 3, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the mechanism places the lift pins at a first predetermined distance above the surface of the wafer platen in the clamp position, the first predetermined distance allowing the workpiece to be clamped to the wafer platen (Lubomirskey et al., paragraph [0003], lines 1-5).

Regarding claim 4, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the mechanism

places the lift pins at a second predetermined distance above the surface of the wafer platen in the lift off position, the second predetermined distance allowing a workpiece removing device to be positioned between the workpiece and the wafer platen without contacting either surface. (Lubomirskey et al., paragraph [0003], lines 8-11 and paragraph [0004], lines 11-13).

Regarding claim 5, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 4, wherein the workpiece removing device comprises a robotic arm (Lubomirskey et al., paragraph [0002], lines 6-16).

Regarding claim 6, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the mechanism comprises a cylinder (Fig. 1,49) for engaging the lift pins in the load, clamp and lift off positions. It would have been obvious to those skilled in the art at the time the invention was made to use a second cylinder instead of a single cylinder used as the mechanism for engaging the lifting pins to control lateral (left or right) movement of the wafer during the loading and removing of the wafer from the wafer platen during the semiconductor process.

Regarding claim 7, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the plurality of lift pins comprise three lift pins (Reichelderfer et al., column 2, lines 36-38).

Regarding claim 8, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the three lift pins are

arranged equally in space around the axis of the platen (Reichelderfer et al., column 2, lines 36-38). It would have been obvious to those skilled in the art at the time the invention was made to have equally spaced the lifting pins in a triangular manner to provide support increased for the workpiece.

Regarding claim 9, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the plurality of lift pins comprise more than three lift pins (Reichelderfer et al., column 2, lines 36-38).

Regarding claims 10, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the lift pins comprises pointed tips (Reichelderfer et al. Fig. 3,51 and column 2, lines 41-45). It would have been obvious to those skilled in the art at the time the invention was made to provide lifting pins comprising pointed tips to minimize the amount of space or surface area where the pins are located on the wafer to provide more accuracy necessary for semiconductor processing, such as ion implantation.

Regarding claims 11, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the locator pins (Reichelderfer et al. Fig. 3,51 and column 2, lines 41-45) comprise flattened tips. It would have been obvious to those skilled in the art at the time the invention was made to provide lifting pins comprising a flattened tip to stabilize the amount of movement of the wafer during the loading, clamping, and lift off stages and also providing a reliable transfer of the wafer during completion of the semiconductor process.

Regarding claim 13, Reichelderfer et al. in view of Lubomirskey et al. discloses an apparatus for handling a workpiece as defined in claim 1, wherein the wafer platen comprises aluminum or ceramic materials (Reichelderfer et al., column 1, lines 54-61).

Regarding claim 14, Reichelderfer et al. in view of Lubomirskey et al. discloses a apparatus for handling a workpiece as defined in claim 1, further comprising a gas cooling controller (Reichelderfer et al., Fig. 3, 38 and column 3,34-38) for cooling a backside chamber between the workpiece and the wafer platen.

Regarding claims 19, Reichelderfer et al. in view of Lubomirskey et al. discloses the claimed method for handling a workpiece during semiconductor processing, comprising the steps of: loading a workpiece on a wafer platen (Lubomirskey et al. paragraph [0002], lines 13-17); engaging lift pins through the channels of the wafer platen above the surface of the wafer platen for positioning the workpiece in a clamping position (Lubomirskey et al., paragraph [0003], lines 1-5); engaging the lift pins through the channels of the wafer to further lift the workpiece above the surface of the wafer platen for positioning the workpiece in a lift off position (Lubomirskey et al., paragraph [0003], lines 5-11).

Regarding claims 20, Reichelderfer et al. in view of Lubomirskey et al. discloses the claimed method for handling a workpiece as defined in claim 1, wherein the lift pins are placed below the surface of the wafer platen during the step of loading, the lift pins are engaged at a first predetermined distance above the surface of the wafer platen in the clamping position with the first predetermined distance allowing the workpiece to be clamped to the wafer platen, and the lift pins are engaged at a second

predetermined distance above the surface of the wafer platen in the lift off position with the second predetermined distance allowing a workpiece removing device to be positioned between the workpiece and the wafer platen without contacting either surface.

4. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichelderfer, et al. (US 5,016,332) and view of Lubomirsky et al. (US 2002/0121312 A1) as applied to claim 1 above, and further in view of Collins et al. (US 6,454,898).

Regarding claim 12, Reichelderfer, et al. in view of Lubomirsky et al. discloses an apparatus for handling a workpiece as defined in claim 1, however they both do not disclose the lift pins comprising tungsten, aluminum, carbide, nitride, graphite or titanium.

However, Collins et al. discloses the lifting pins comprising silicon carbide (column 32, lines 37-47). It would have been obvious to those skilled in the art at the time the invention was made to have modified the handling apparatus of Reichelderfer, et al. in view of Lubomirsky et al. by providing silicon carbide lifting pins taught by Collins et al. to provide a higher resistivity for the biasing wafer and therefore do not pose a greater risk for arcing during the semiconductor processing.

Regarding claim 17, Reichelderfer, et al. in view of Lubomirsky et al. discloses an apparatus for handling a workpiece as defined in claim 1, however they both do not disclose a bias source for supplying a bias voltage to the lift pins.

However, Collins et al. discloses a bias source (Fig. 26, 1420) for supplying a bias voltage to the lift pins (Fig. 27, 4010). It would have been obvious to those skilled in the art at the time the invention was made to have modified the handling apparatus of Reichelderfer, et al. in view of Lubomirsky et al. by providing a bias source for supplying a bias voltage taught by Collins et al. to the lifting pins taught by Reichelderfer et al. and Lubomirsky et al. to provide a higher resistivity for the biasing wafer and therefore decrease the risk of arcing during the semiconductor processing.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reichelderfer, et al. (US 5,016,332) and view of Lubomirsky et al. (US 2002/0121312 A1) as applied to claim 14 above, and further in view of Krueger (US 5,131,460).

Regarding claim 15, Reichelderfer, et al. in view of Lubomirsky et al. discloses an apparatus for handling a workpiece as defined in claim 14, however they both do not disclose a gas source cooling controller comprises a gas source for supplying gas to the backside chamber, a pressure controller for regulating the pressure of the gas supplied to the backside chamber, an exhaust pump for exhausting gas from the backside chamber and a switch for switching between supplying gas and exhausting gas through a gas feed through in the wafer platen.

However, Krueger discloses an apparatus for semiconductor fabrication wherein the gas cooling controller comprises a gas source (Fig. 2, 46) for supplying gas to the backside chamber (column 4, lines 16-24), a pressure controller for regulating the pressure of the gas supplied to the backside chamber (abstract, lines 1-8), an exhaust pump (Fig. 2, 60) for exhausting gas from the backside chamber and a switch (Fig. 2,

42 and 44 and column 4, lines 33-66) for switching between supplying gas and exhausting gas through a gas feed through in the wafer platen (Fig. 2, 20). It would have been obvious to those skilled in the art at the time the invention was made to have modified the gas cooling controller taught by Reichelderfer, et al. and Lubomirsky et al. by providing a gas source, pressure controller, a exhaust pump and a switch taught by Krueger to control the amount of gas and pressure following through the backside chamber of the semiconductor device thereby eliminating vibration and contamination of semiconductor devices due to unwanted particulates on the semiconductor substrates.

6. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichelderfer, et al. (US 5,016,332) and view of Lubomirsky et al. (US 2002/0121312 A1) as applied to claim 1 above, and further in view of Wicker et al. (US 4,724,510).

Regarding claim 16, Reichelderfer, et al. in view of Lubomirsky et al. discloses an apparatus for handling a workpiece as defined in claim 1, however they both do not disclose a plurality of electrical contacts on the top surface of the wafer platen.

However, Wicker et al. discloses a wafer handling for an electrostatic clamp for holding a semiconductor wafer comprising a plurality of electrical contracts (Fig. 6, 25 and 27) on the top surface of the wafer platen (Fig. 6, 20 and 30). It would have been obvious to those skilled in the art at the time the invention was made to provide a plurality of electrical contact pins on the top surface of the wafer platen taught by Wicker et al. to the handling apparatus of Reichelderfer, et al. and Lubomirsky et al. to serve both as electrical contacts to the electrodes as well as to facilitate mechanical

positioning of the clamp, therefore providing good thermal conductivity for the electrostatic wafer clamp.

Regarding claim 18, Reichelderfer, et al. in view of Lubomirsky et al. and in further view of Wicker et al. discloses an apparatus for handling a workpiece as defined in claim 16, comprising a bias source for supplying a bias voltage to the lift pins and the electrical contracts (Wicker et al., column 3, lines 27-44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRW

PHUONG T. VU
PRIMARY EXAMINER